ABSTRACT OF THE DISCLOSURE

A ferroelectric memory capable of suppressing false data reading or the like by increasing a read margin is obtained. This ferroelectric memory comprises a circuit applying a read voltage $V_R$ to a first electrode and a detector capable of detecting the difference between electric capacitances $C_{f0}$ and $C_{f1}$ of a ferroelectric film when the potential difference of a second electrode corresponding to the difference between the electric capacitances $C_{f0}$ and $C_{f1}$ of the ferroelectric film is in excess of a detection limit voltage $V_S$. The electric capacitance $C_2$ of the second electrode is set to satisfy the following expression:

$$C_{f0} < C_2 \leqq 1/2 \times \{(C_{f1} - C_{f0})V_R/V_S - (C_{f1} + C_{f0})\}$$